36. (Amended) A semiconductor integrated circuit comprising a receiving circuit for receiving a transmission signal, which is behind a standard timing signal by a predetermined delay time in accordance to a logical value,

for detecting a delay time between a transition edge of the transmission signal transmitting through a signal line, and the transition edge of the standard timing signal, and

for generating the logical value according to the detected delay time.

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A marked-up version of the amended claims is enclosed as required by 37 C.F.R. § 1.121.